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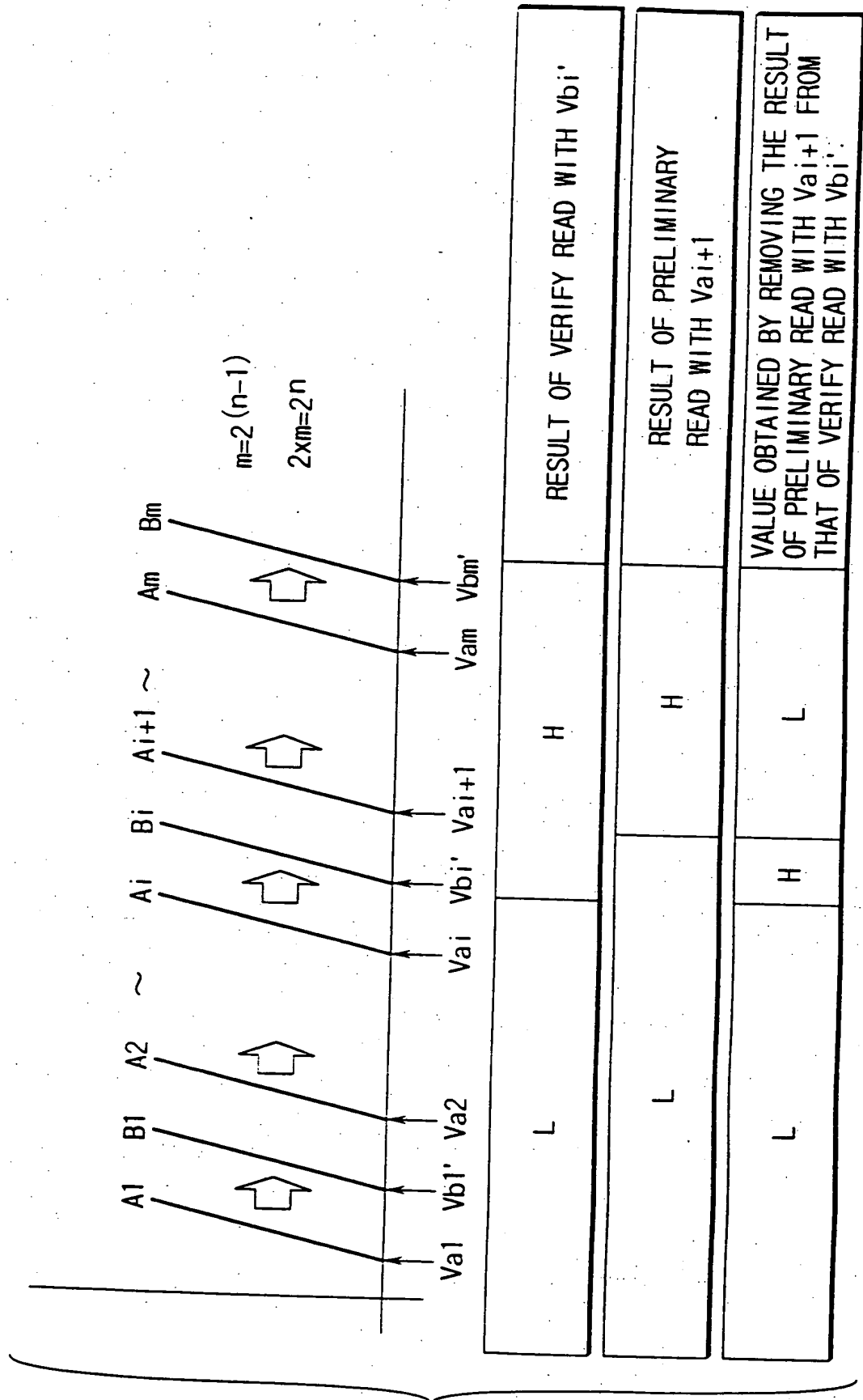


FIG.1

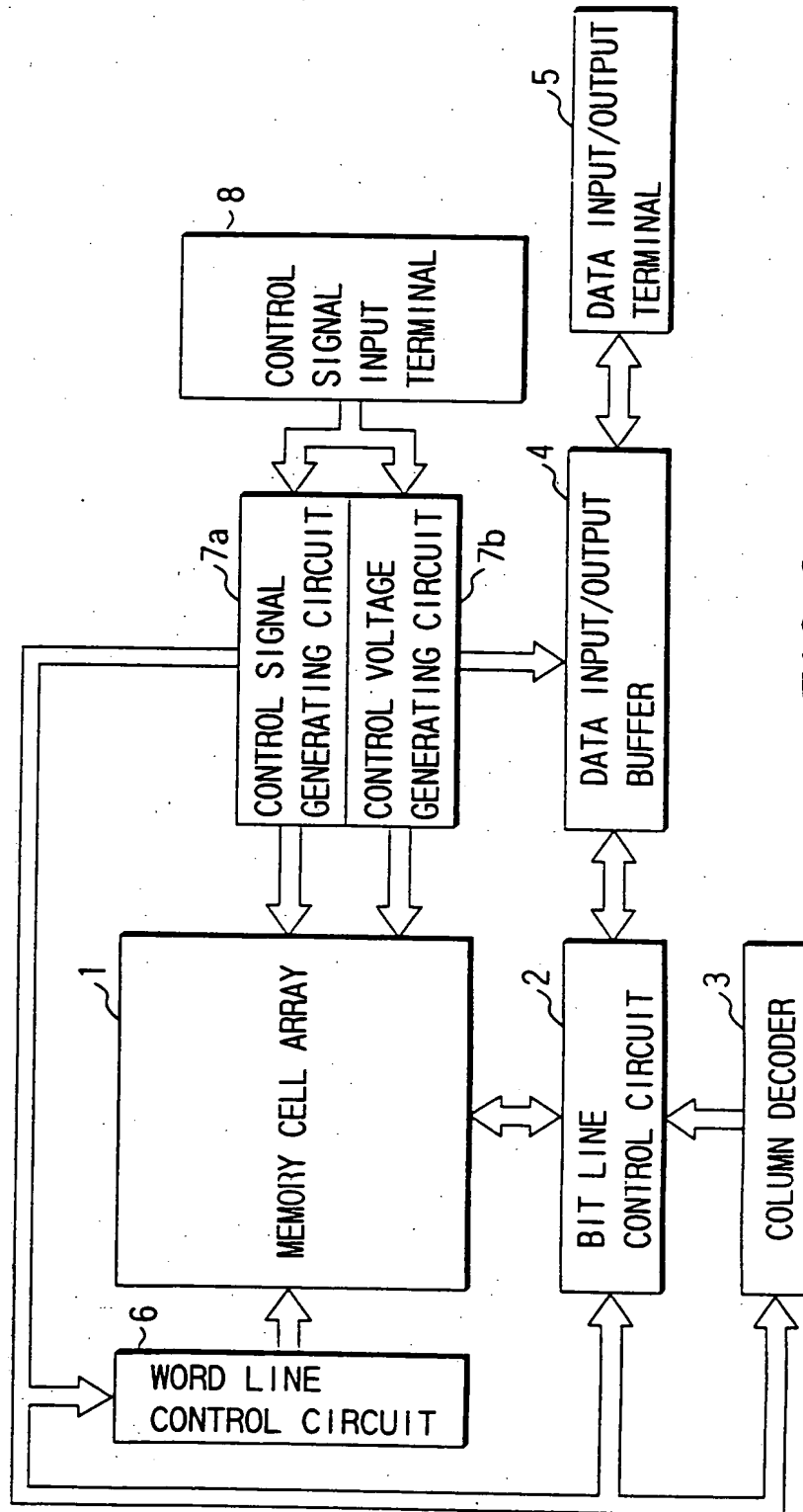


FIG. 2

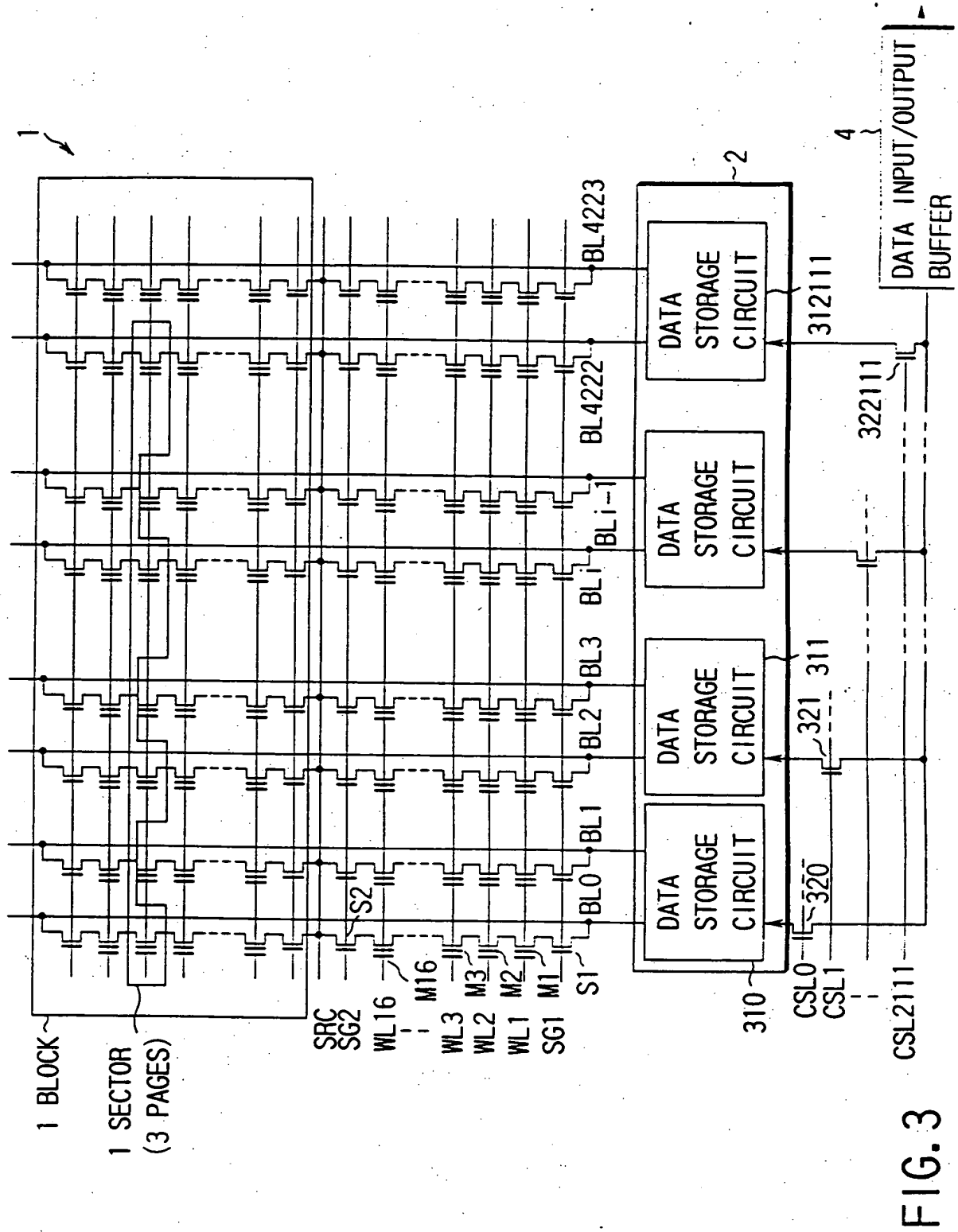
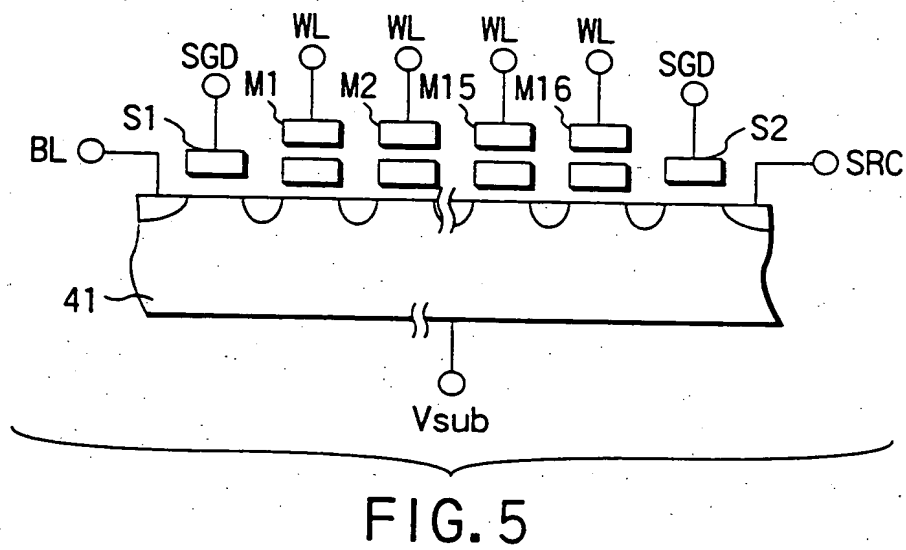
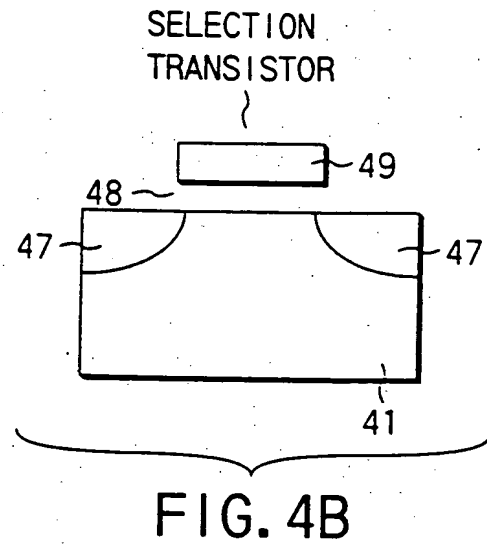
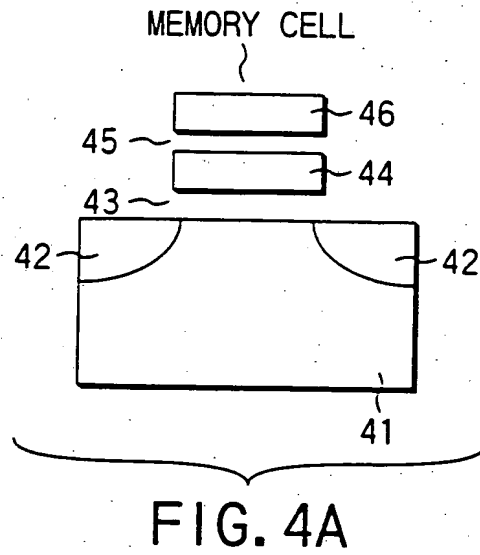
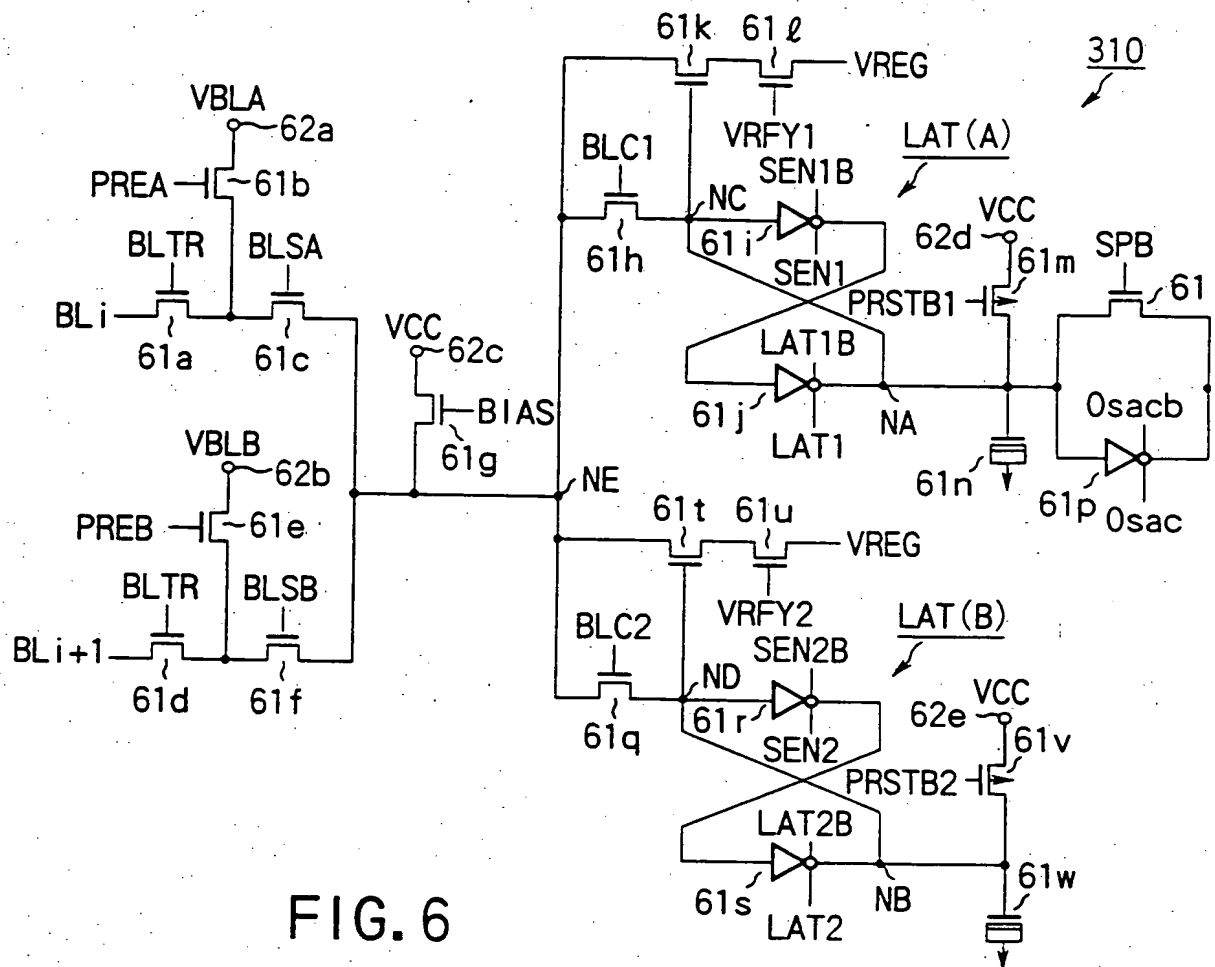


FIG. 3





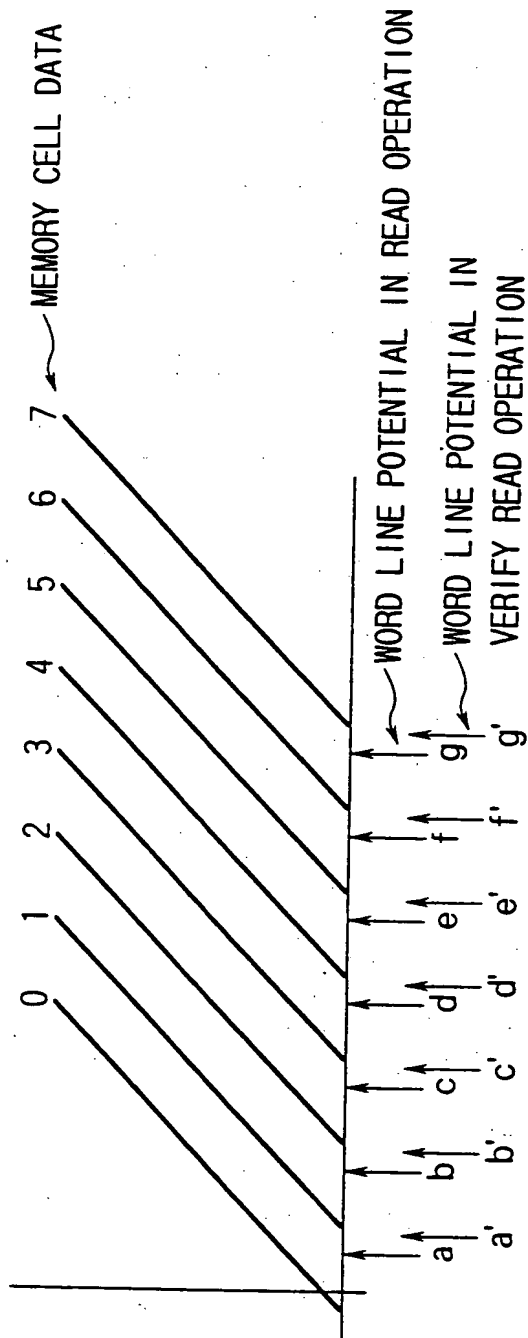


FIG.7

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	DATA TO BE WRITTEN AND READ		
		1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN 0V	1	1	1
1	0.3V~0.5V	1	1	0
2	0.8V~1.0V	1	0	1
3	1.3V~1.5V	1	0	0
4	1.8V~2.0V	0	1	1
5	2.3V~2.5V	0	1	0
6	2.8V~3.0V	0	0	1
7	3.3V~3.5V	0	0	0

FIG.8



Fig. 9.

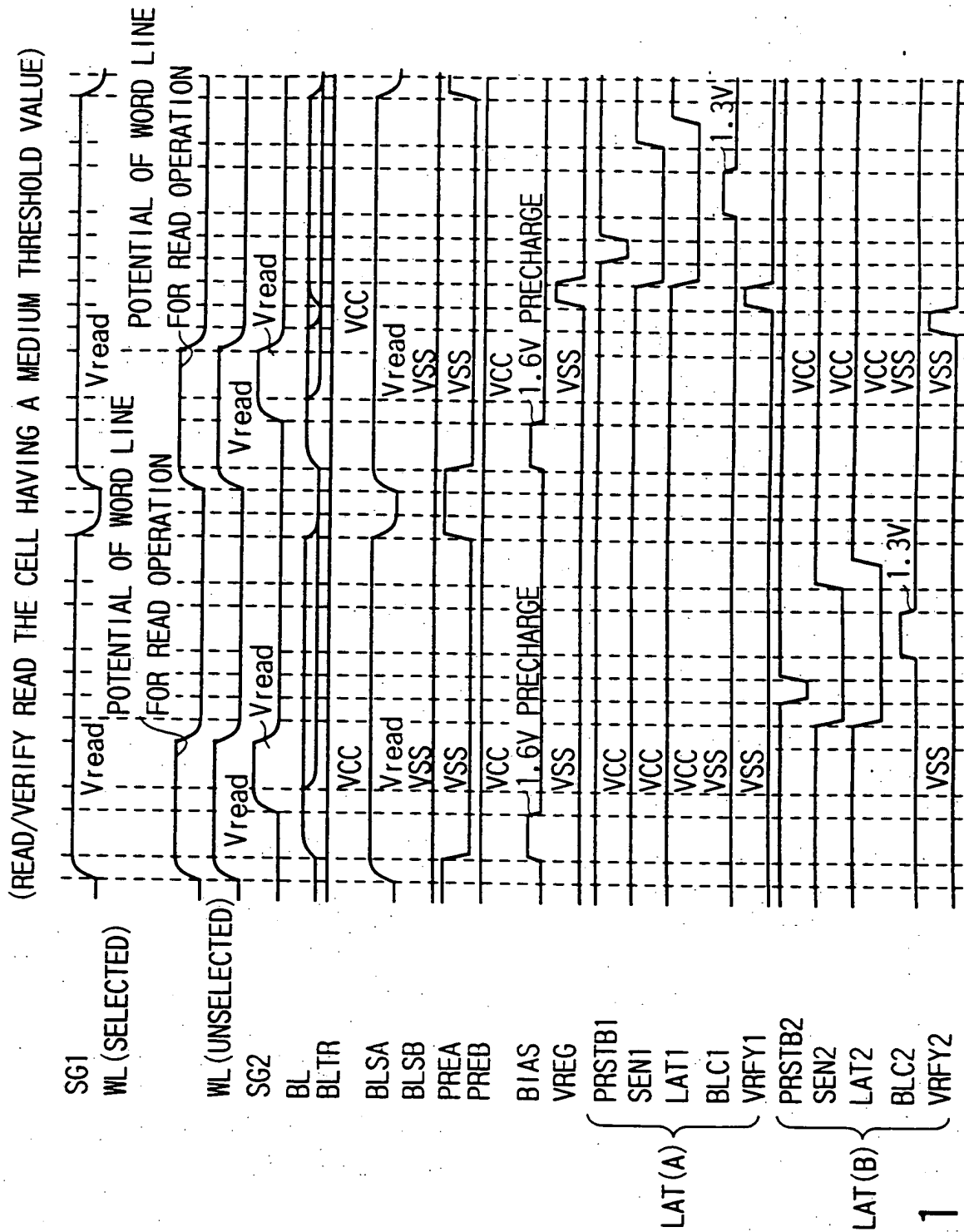


FIG. 11

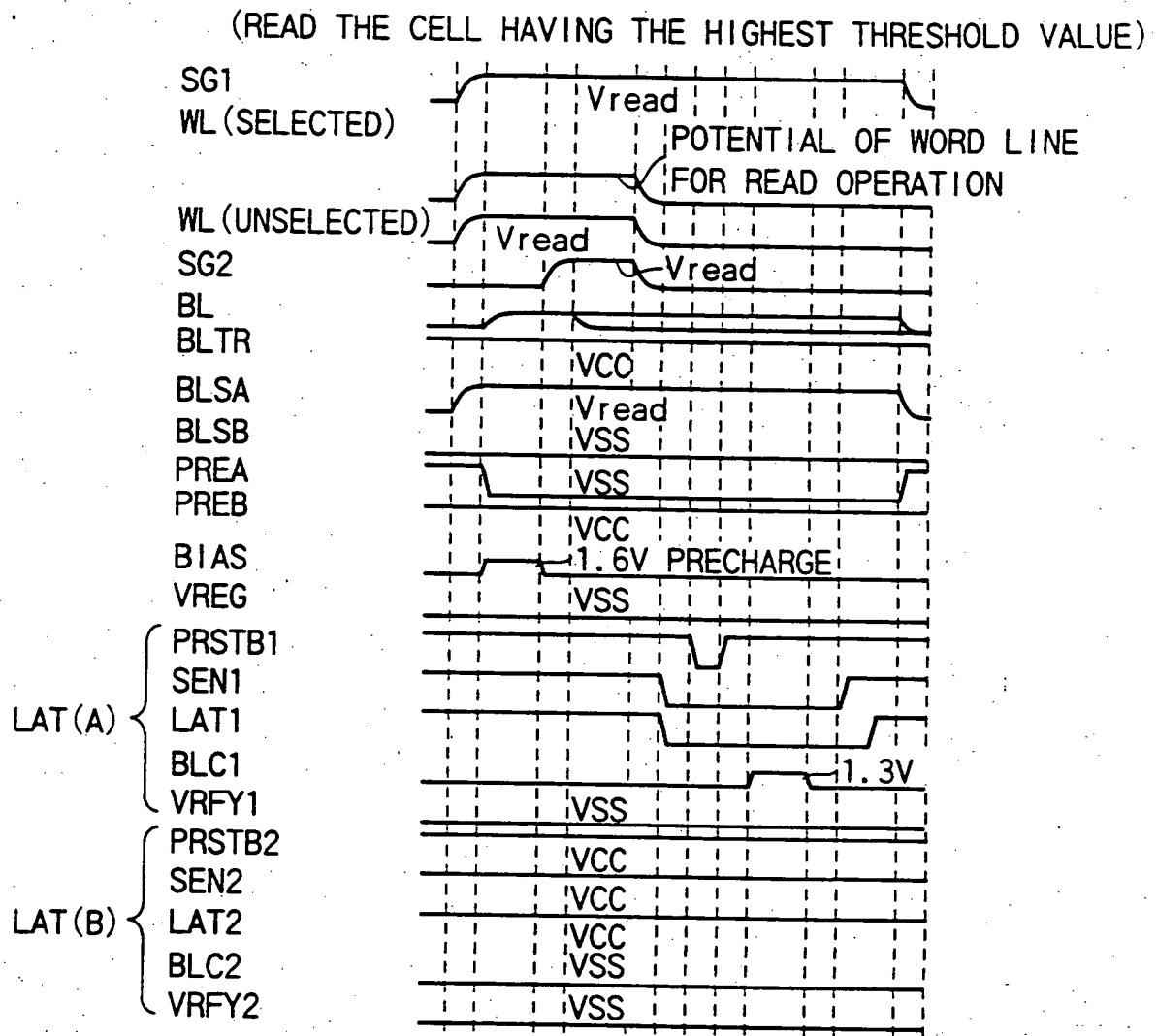


FIG. 12

FIG. 13A

PROG. VERIFY (1st PAGE)

MEMORY CELL DATA			
0 → 4			
INHIBIT	WRITE(OK)	WRITE(NG)	
A B BIT	A B BIT	A B BIT	
H	L	L	A=LAT(A), B=LAT(B), BIT=BL
H	L	L	DATA LOADING (WRITE → L, INHIBIT → H FOR A)
H	L	L	READ AT 'd'
H	H	L	BIT LINE IS AT H WHEN A IS H (VRFY1)
H	H	L	POTENTIAL OF BIT LINE IS APPLIED TO A
H	H	L	0 → 4 VERIFY

PROG. VERIFY (2nd PAGE)

MEMORY CELL DATA			
0 → 2			
INHIBIT	WRITE(OK)	WRITE(NG)	
A B BIT	A B BIT	A B BIT	
H	L	L	4 → 6 VERIFY
H	L	L	A=LAT(A), B=LAT(B), BIT=BL
H	L	L	DATA LOADING (WRITE → L, INHIBIT → H FOR A)
H	L	L	READ AT 'f'
H	L	L	BIT LINE IS AT H WHEN A IS H (VRFY1)
H	L	L	POTENTIAL OF BIT LINE IS APPLIED TO A

FIG. 13B

PROG. VERIFY (2nd PAGE)

DATA LOADING			
0 → 2 VERIFY			
INHIBIT	WRITE(OK)	WRITE(NG)	
A B BIT	A B BIT	A B BIT	
H	L	L	READ AT 'd'
H	L	L	POTENTIAL OF BIT LINE IS APPLIED TO B
H	L	L	(FIRST TIME OF LOOP)
H	L	L	READ AT 'b'
H	L	L	BIT LINE IS AT L WHEN B IS H (VRFY2)
H	L	L	BIT LINE IS AT H WHEN A IS H (VRFY1)
H	L	L	POTENTIAL OF BIT LINE IS APPLIED TO A

FIG. 13C

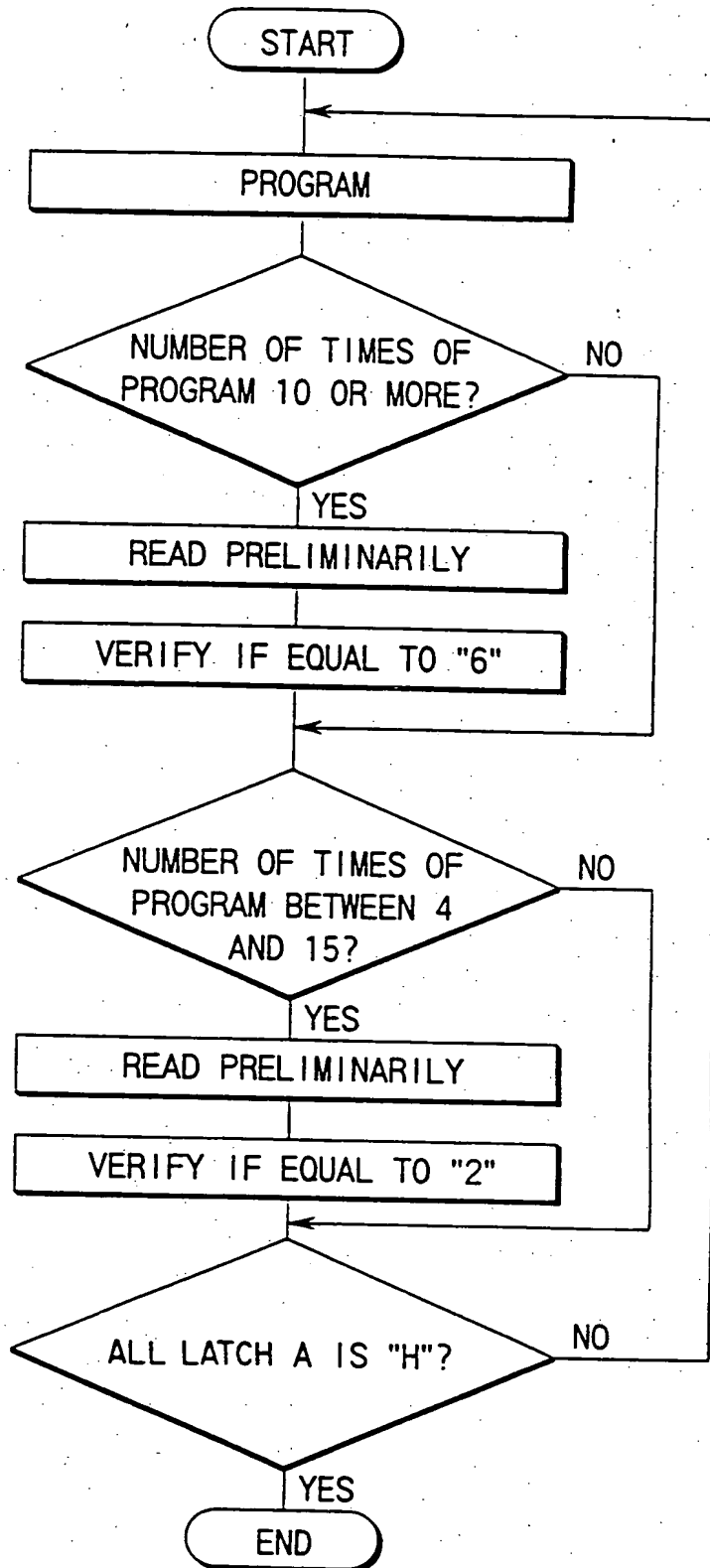


FIG. 13D

PROG. VERIFY (3rd PAGE)

0		0→1		2		2→3		4		4→5			
INHIBIT A B BIT		WRITE(OK) A B BIT		WRITE(NG) A B BIT		INHIBIT A B BIT		WRITE(OK) A B BIT		WRITE(NG) A B BIT		INHIBIT A B BIT	
H		L		H		L		H		L		L	
H		L		H		L		H		L		L	
H		L		H		L		H		L		L	
H		L		H		L		H		L		L	

FIG. 14A

6		6→7		MEMORY CELL DATA	
INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	INHIBIT A B BIT	INHIBIT A B BIT	WRITE(OK) A B BIT
H	L	L	L	L	L
H	L	L	L	L	L
H	L	L	L	L	L
H	L	L	L	L	L

FIG. 14B

[illegible]

6	6→7	MEMORY CELL DATA
H	L	DATA LOADING (WRITE→L, INHIBIT→H FOR A)
H	L	READ AT f
H	H	POTENTIAL OF BIT LINE IS APPLIED TO B
H	H	READ AT e'
H	L	BIT LINE IS AT L WHEN B IS H (VRFY2)
H	H	BIT LINE IS AT H WHEN A IS H (VRFY1)
H	H	POTENTIAL OF BIT LINE IS APPLIED TO A

$$A = \text{LAT}(A), \quad B = \text{LAT}(B)$$

FIG. 16A

[illegible]

FIG. 16B

6	6→7	MEMORY CELL DATA	
H	L	DATA LOADING	
H	H	<div style="display: flex; align-items: center; justify-content: center;"> <div style="width: 50%; height: 100%; background: linear-gradient(to top right, transparent 49%, black 49%, black 51%, transparent 51%);"></div> <div style="width: 50%; height: 100%; background: linear-gradient(to bottom right, transparent 49%, black 49%, black 51%, transparent 51%);"></div> </div>	2→3 VERIFY
H	H		READ AT d POTENTIAL OF BIT LINE IS APPLIED TO B
H	H		READ AT c' BIT LINE IS AT L WHEN B IS H (VRFY2)
H	H		BIT LINE IS AT H WHEN A IS H (VRFY1)
H	H		POTENTIAL OF BIT LINE IS APPLIED TO A
H	H		

$$A = \text{LAT}(A), \quad B = \text{LAT}(B)$$

PROG. VERIFY (3rd PAGE)

0	0→1		2	2→3		4	4→5	
H	L	L	H	L	H	L	L	L
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H
H	L	L	H	L	H	H	L	H

FIG.17A

PROG. VERIFY (3rd PAGE)

6	6→7		MEMORY CELL DATA		0→1	
H	L	L	DATA LOADING		VERIFY	
H	L	L	READ AT b		POTENTIAL OF BIT LINE IS APPLIED TO B	
H	L	L	READ AT a'		POTENTIAL OF BIT LINE IS APPLIED TO A	
H	L	L	BIT LINE IS AT L WHEN B IS H (VRFY2)			
H	L	L	BIT LINE IS AT H WHEN A IS H (VRFY1)			
H	L	L	POTENTIAL OF BIT LINE IS APPLIED TO A			

FIG.17B A=LAT(A), B=LAT(B)

READ (1st PAGE)

0,1,2,3	4,5,6,7
A B BIT	A B BIT
L	H
L	H
A=LAT(A), B=LAT(B), BIT=BL	
READ AT d	
POTENTIAL OF BITI LINE IS APPLIED TO A	
01234567	
READ	

FIG.18A

READ (2nd PAGE)

0,1	2,3	4,5	6,7
A B BIT	A B BIT	A B BIT	A B BIT
L	L	L	H
L	L	L	H
A=LAT(A), B=LAT(B), BIT=BL			
READ AT f			
POTENTIAL OF BITI LINE IS APPLIED TO A			
45,67 READ			

FIG.18B

READ (2nd PAGE)

L	L	L	L	L	H	H	READ AT d	01,23 READ
L	L	L	L	L	H	H	POTENTIAL OF BIT LINE IS APPLIED TO B	
L	L	L	L	L	H	H	READ AT b	
L	L	L	L	L	H	H	BIT LINE IS AT L WHEN B IS H (VRFY2)	
L	L	L	L	L	H	H	BIT LINE IS AT H WHEN A IS H (VRFY1)	
L	L	L	L	L	H	H	POTENTIAL OF BIT LINE IS APPLIED TO A	

FIG.18C

FIG. 19D

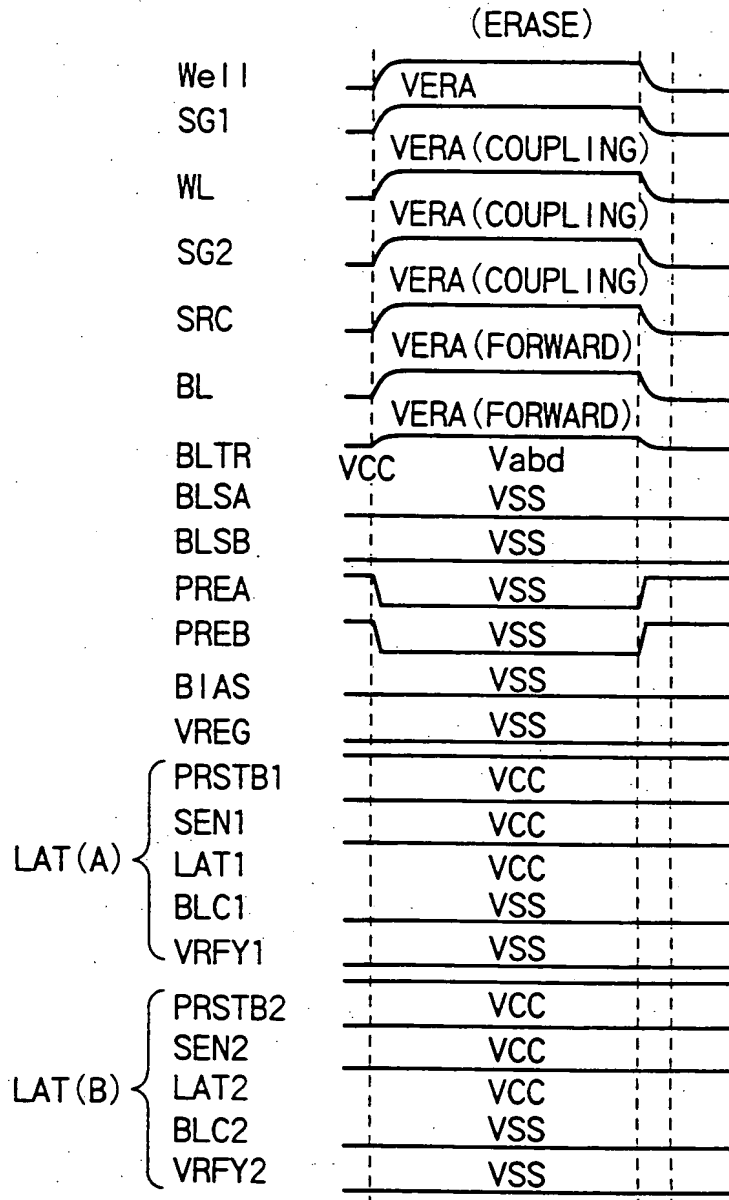


FIG. 20

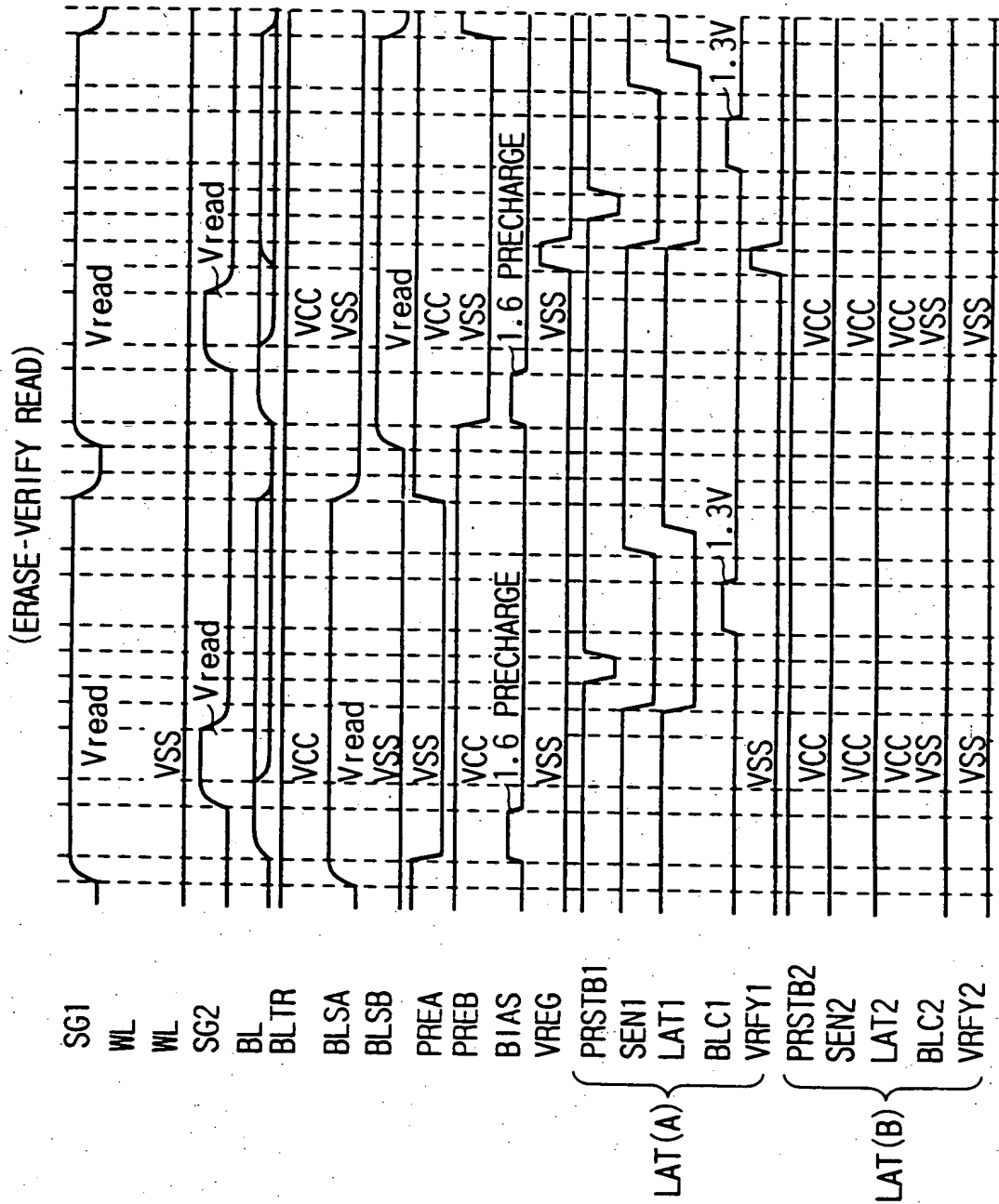


FIG.21

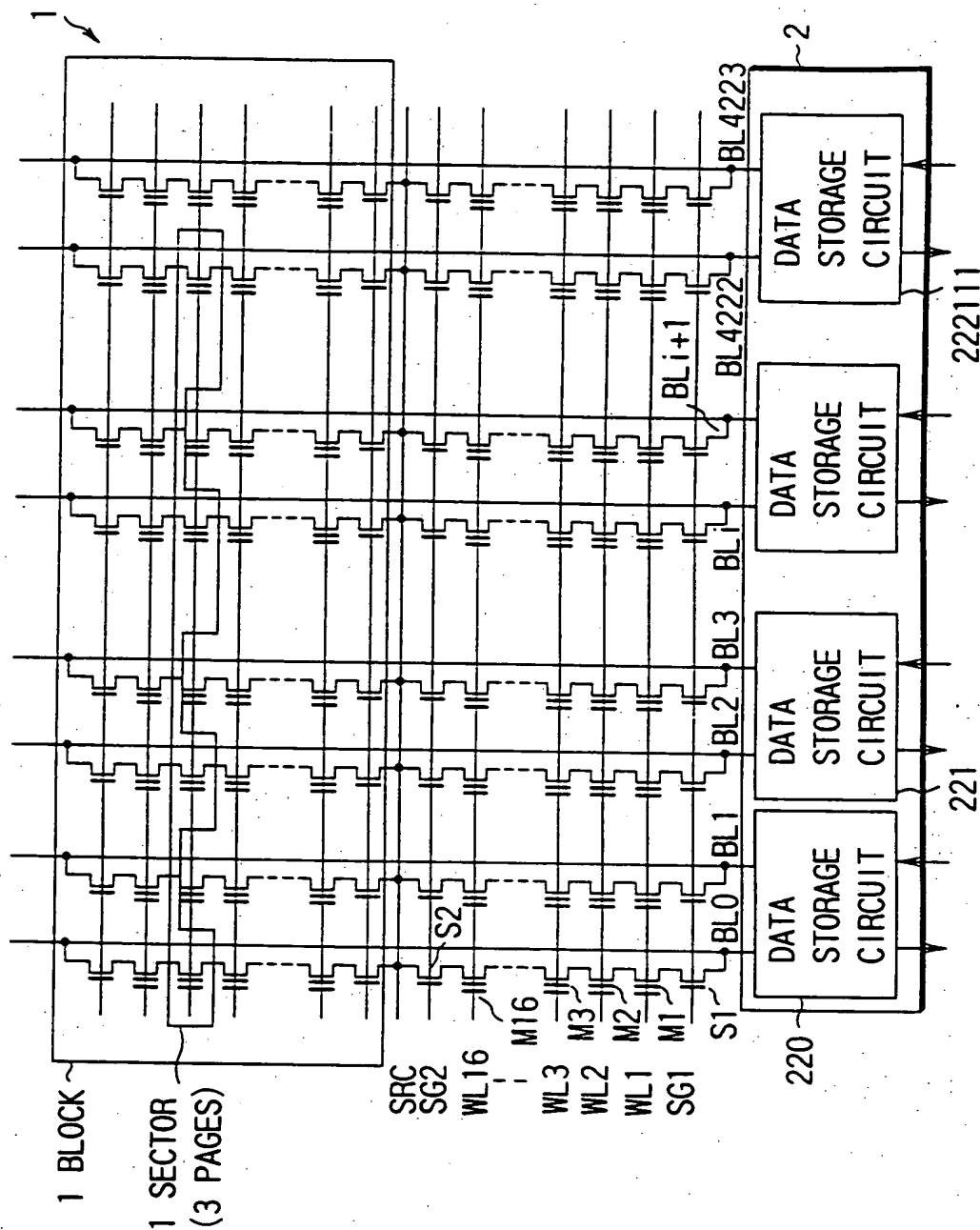
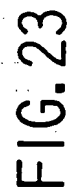


FIG. 22



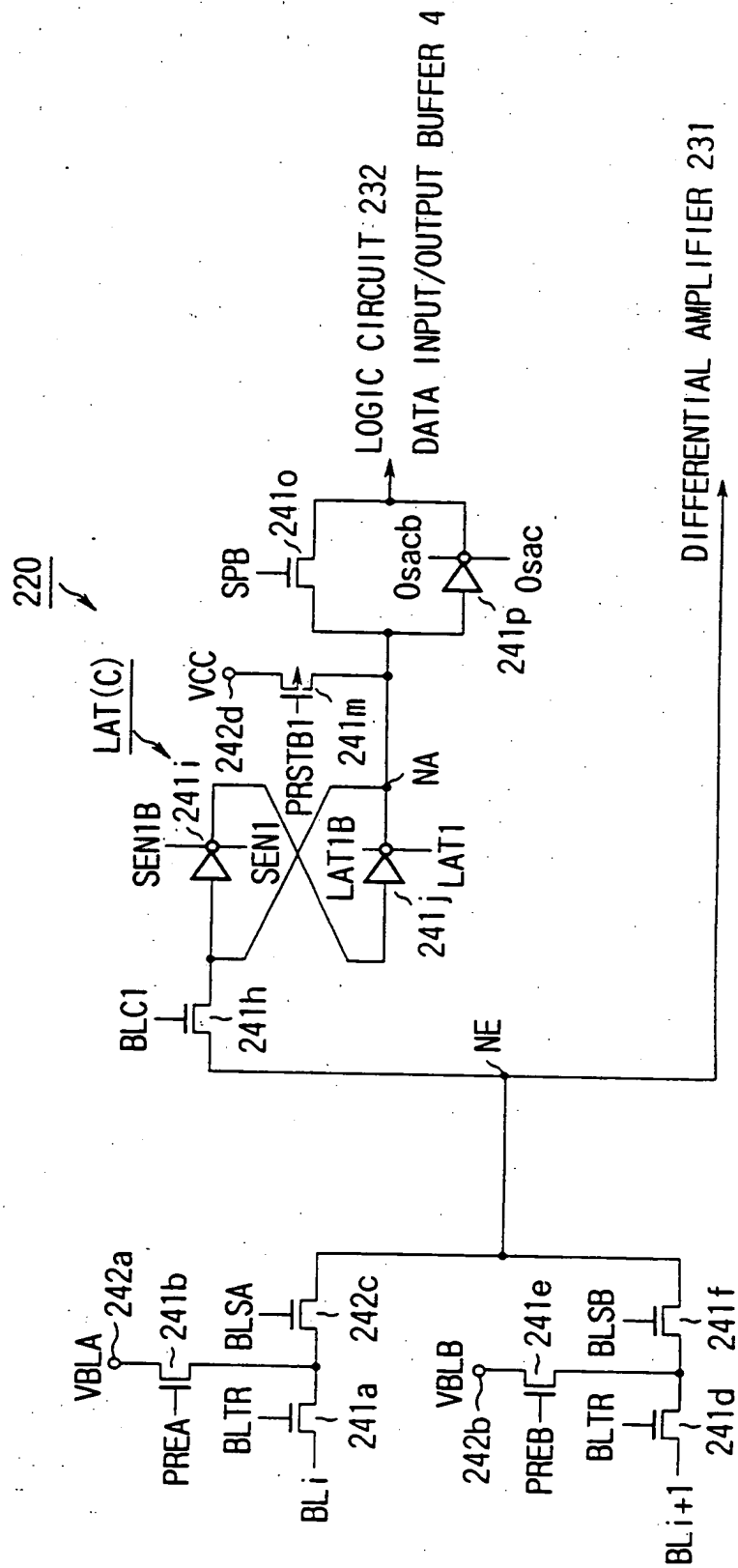


FIG. 24

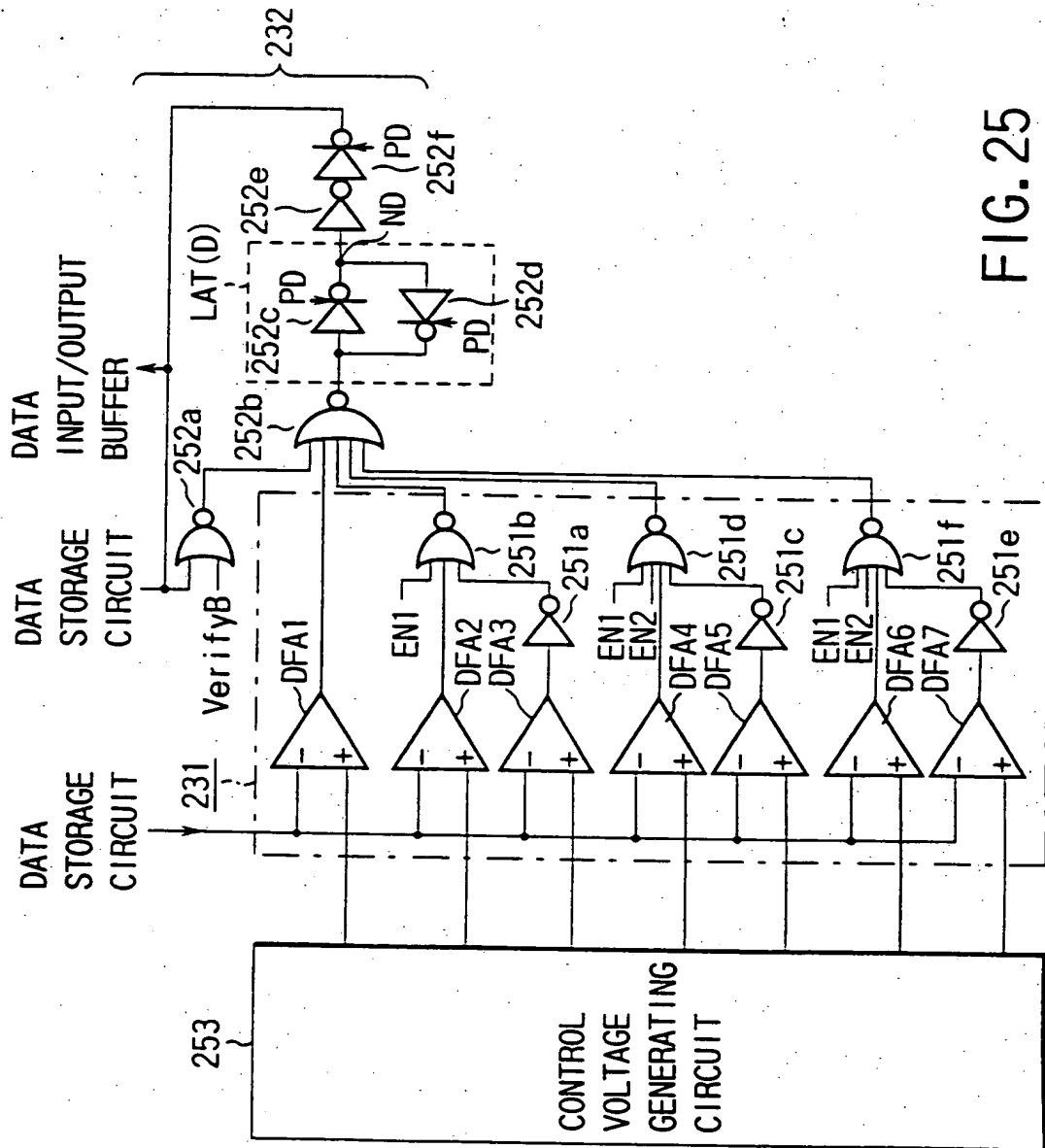


FIG. 25

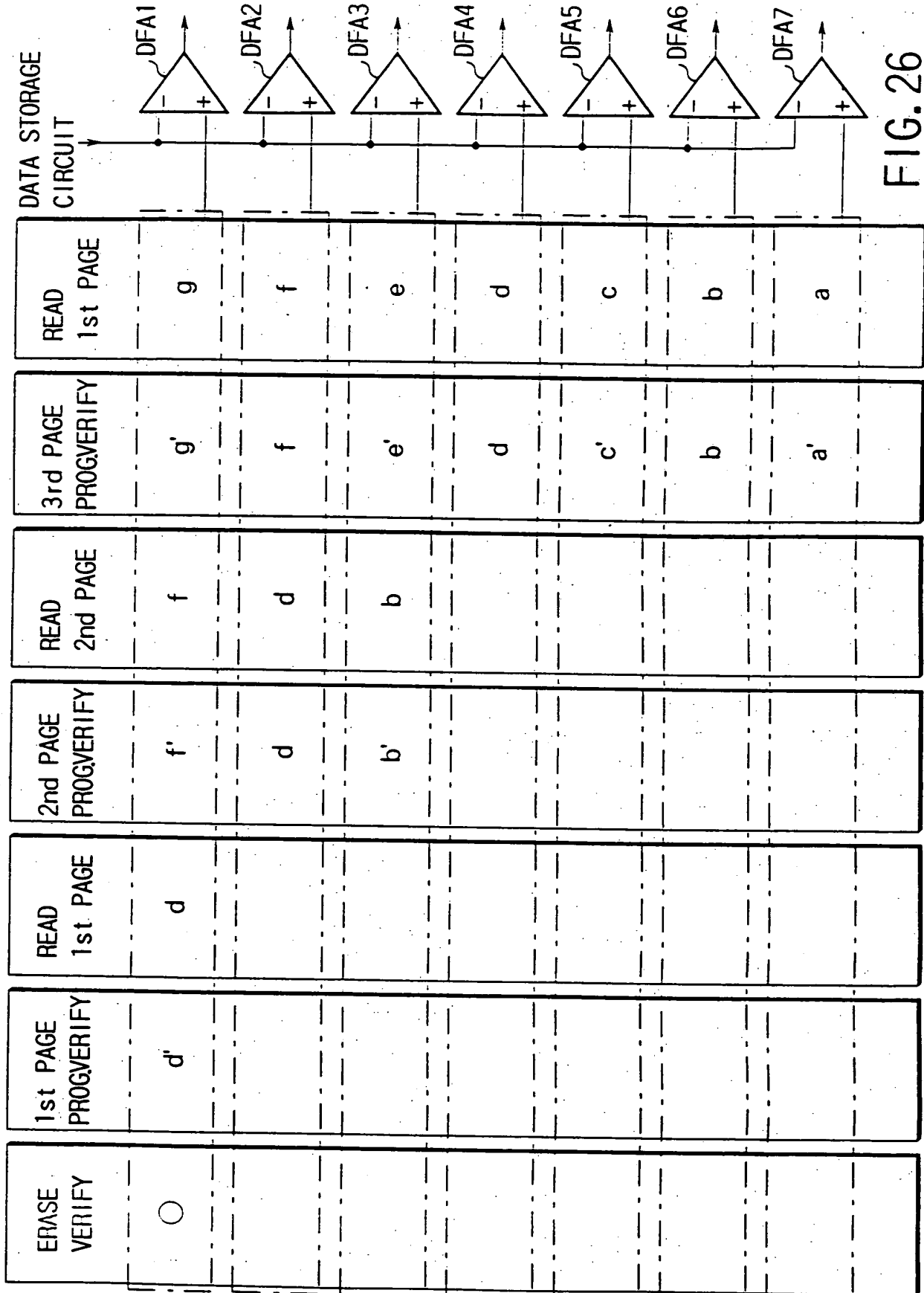


FIG. 26

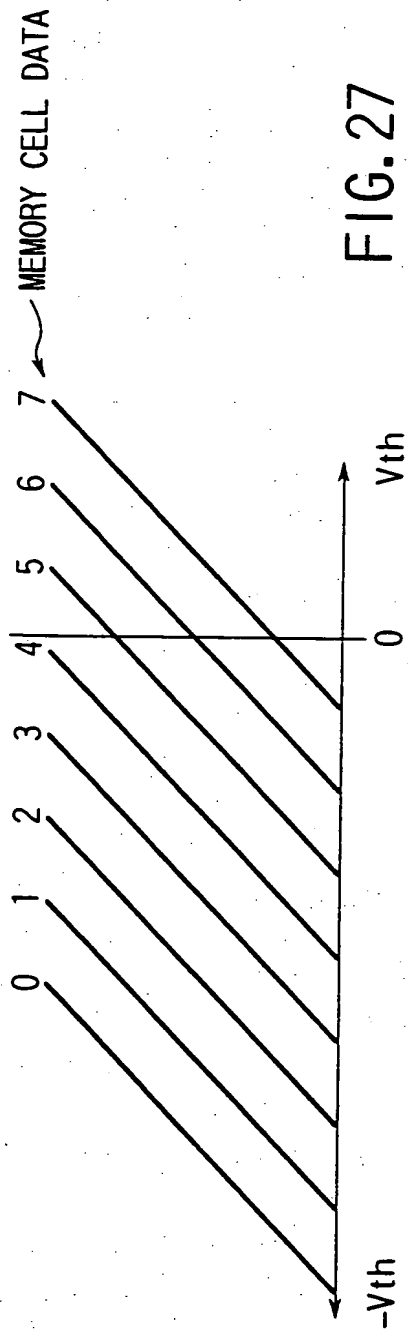


FIG. 27

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	VOLTAGE READ OUT TO BIT LINE	DATA TO BE WRITTEN AND READ		
			1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN -3.8V	3.8V~4.0V	1	1	1
1	-3.5V~-3.3V	3.3V~3.5V	1	1	0
2	-3.0V~-2.8V	2.8V~3.0V	1	0	1
3	-2.5V~-2.3V	2.3V~2.5V	1	0	0
4	-2.0V~-1.8V	1.8V~2.0V	0	1	1
5	-1.5V~-1.3V	1.3V~1.5V	0	1	0
6	-1.0V~-0.8V	0.8V~1.0V	0	0	1
7	-0.5V~-0.3V	0.3V~0.5V	0	0	0

FIG. 28

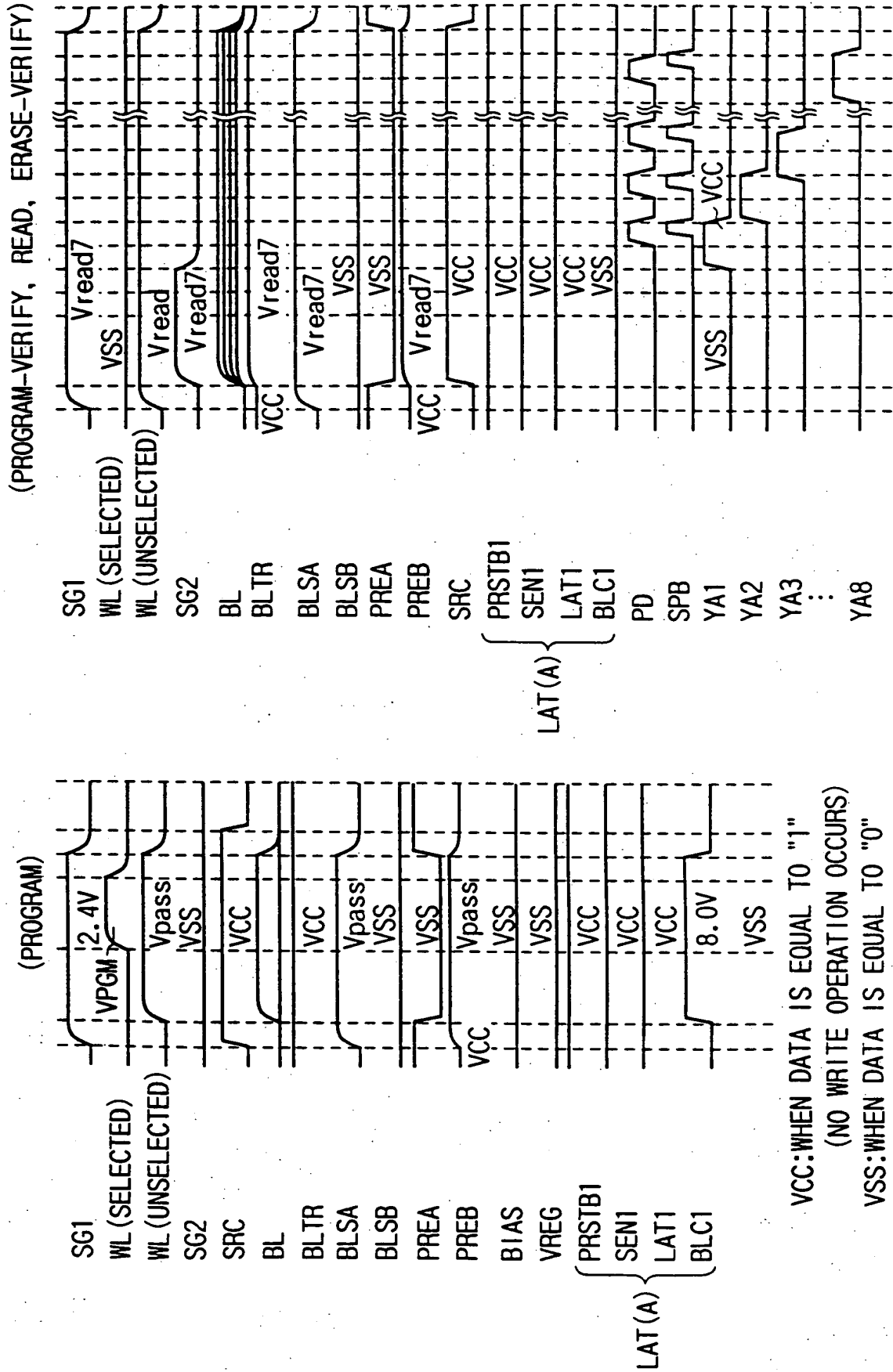


FIG. 29

FIG. 30

REFERENCE POTENTIAL				
READ TIME		PROGRAM-VERIFY TIME		ERASE-VERIFY TIME
a	3.6V	a'	3.5V	○ 4.0V
b	3.1V	b'	3.0V	
c	2.6V	c'	2.5V	
d	2.1V	d'	2.0V	
e	1.6V	e'	1.5V	
f	1.1V	f'	1.0V	
g	0.6V	g'	0.5V	

FIG. 31

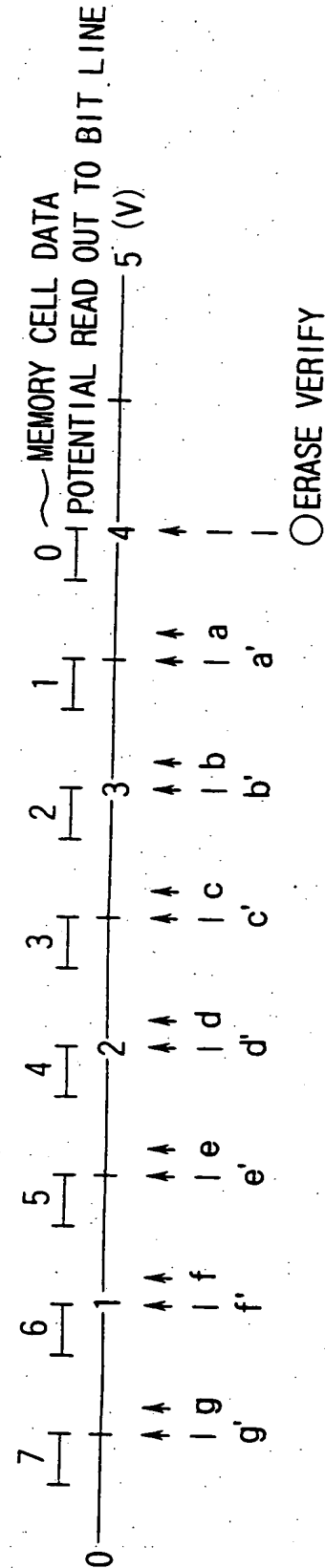


FIG. 32

VERIFY-1st PAGE		
POTENTIAL READ OUT TO BIT LINE	DFA1	LATCHED DATA
NOT HIGHER THAN d'	H	H
NOT LOWER THAN d'	L	L

FIG. 33A

VERIFY-2nd PAGE				
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	LATCHED DATA
NOT HIGHER THAN f'	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN f'	L	H	H	L
NOT HIGHER THAN b' AND NOT LOWER THAN d	L	L	H	H
NOT LOWER THAN b'	L	L	L	L

FIG. 33B

VERIFY-3rd PAGE							
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	DFA4	DFA5	DFA6	LATCHED DATA
NOT HIGHER THAN g'	H	H	H	H	H	H	H
NOT HIGHER THAN f AND NOT LOWER THAN g'	L	H	H	H	H	H	L
NOT HIGHER THAN e' AND NOT LOWER THAN f	L	L	H	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN e'	L	L	L	H	H	H	L
NOT HIGHER THAN c' AND NOT LOWER THAN d	L	L	L	L	H	H	H
NOT HIGHER THAN b AND NOT LOWER THAN c'	L	L	L	L	L	H	L
NOT HIGHER THAN a' AND NOT LOWER THAN b	L	L	L	L	L	L	H
NOT LOWER THAN a'	L	L	L	L	L	L	L

FIG. 33C

READ-1st PAGE		
POTENTIAL READ OUT TO BIT LINE	DFA1	LATCHED DATA
NOT HIGHER THAN d	H	H
NOT LOWER THAN d	L	L

FIG. 34A

READ-2nd PAGE				
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	LATCHED DATA
NOT HIGHER THAN f'	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN f	L	H	H	L
NOT HIGHER THAN b AND NOT LOWER THAN d	L	L	H	H
NOT LOWER THAN b	L	L	L	L

FIG. 34B

READ-3rd PAGE							
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	DFA4	DFA5	DFA6	LATCHED DATA
NOT HIGHER THAN g	H	H	H	H	H	H	H
NOT HIGHER THAN f AND NOT LOWER THAN g	L	H	H	H	H	H	L
NOT HIGHER THAN e AND NOT LOWER THAN f	L	L	H	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN e	L	L	L	H	H	H	L
NOT HIGHER THAN c AND NOT LOWER THAN d	L	L	L	L	H	H	H
NOT HIGHER THAN b AND NOT LOWER THAN c	L	L	L	L	L	L	L
NOT HIGHER THAN a AND NOT LOWER THAN b	L	L	L	L	L	L	H
NOT LOWER THAN a	L	L	L	L	L	L	L

FIG. 34C

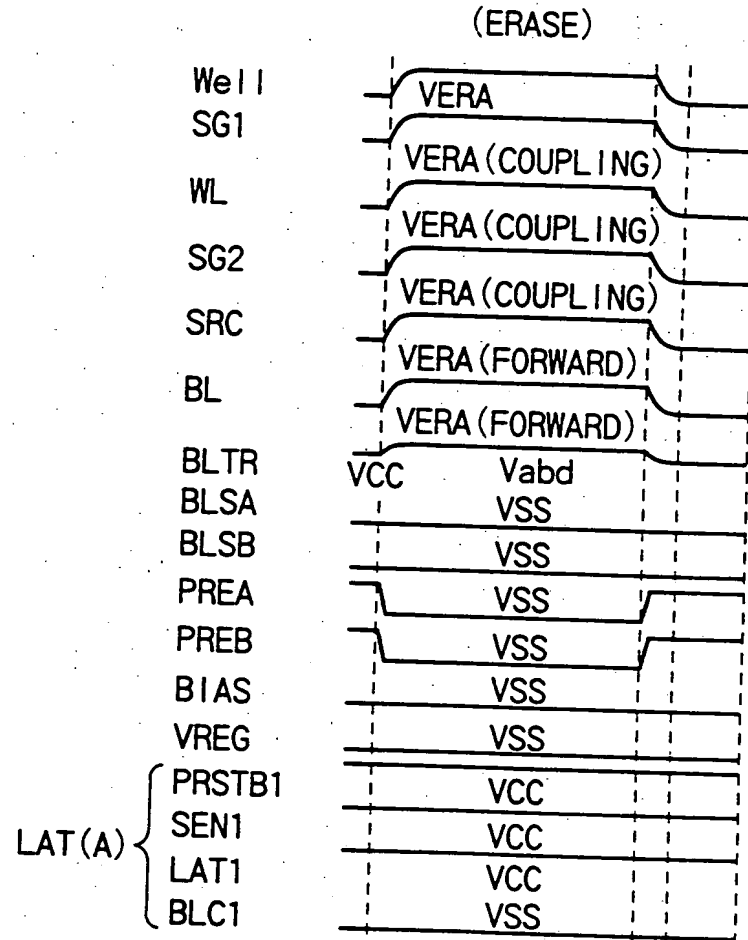


FIG. 35

FIG. 36

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	EXTERNALLY INPUT DATA TO BE WRITTEN AND DATA TO BE READ			DATA OF LAT (A) BEING WRITTEN 0→A WRITE OPERATION OCCURS 1→NO WRITE OPERATION OCCURS		
		1st PAGE	2nd PAGE	3rd PAGE	1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN 0V	1	1	1	1	1	1
1	0.3V~0.5V	1	1	0	1	1	0
2	0.8V~1.0V	1	0	0	1	0	1
3	1.3V~1.5V	1	0	1	1	0	0
4	1.8V~2.0V	0	0	1	0	1	1
5	2.3V~2.5V	0	0	0	0	1	0
6	2.8V~3.0V	0	1	0	0	0	1
7	3.3V~3.5V	0	1	1	0	0	0

(2nd PAGE)

0		0→2		4		4→6		MEMORY CELL DATA	
A	B	A	B	A	B	A	B	A=LAT(A), B=LAT(B), BIT=BL	
H		L		L		H		EXTERNAL DATA LOADING	
H	L	L	L	L	L	H	H	READ AT d	
H	L	L	L	L	L	H	H	POTENTIAL OF BIT LINE IS APPLIED TO B	
H	L	L	L	L	L	H	L	BIT LINE IS AT L WHEN A IS H	
H	L	L	L	L	L	L	L	A IS AT L WHEN B IS AT H	
H	L	L	L	L	L	L	L	BIT LINE IS AT H WHEN A IS H	
H	L	L	L	L	L	L	L	POTENTIAL OF BIT LINE IS APPLIED TO A	
H	L	L	L	L	L	L	L	USE SUBSEQUENT VALUE OF A AS DATA TO BE WRITTEN	

FIG. 37

(3rd PAGE) (INTERNAL DATA CONVERSION)

0	0→1	2	2→3	4	4→5	6	6→7	MEMORY CELL DATA
A B BITA	B BITA	B BITA	B BITA	B BITA	A B BITA	A B BITA	A B BITA	A=LAT(A), B=LAT(B), BIT=BL
H	L	L	H	H	L	L	H	EXTERNAL DATA LOADING
H	L	L	H	H	L	L	H	READ AT f
H	L	L	H	H	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO B
H	L	L	H	H	L	L	H	READ AT d
H	L	L	H	H	L	L	H	BIT LINE IS AT L WHEN B IS AT H
H	L	L	H	H	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO B
H	L	L	H	H	L	L	H	READ AT b
H	L	L	H	H	L	L	H	BIT LINE IS AT H WHEN B IS AT H
H	L	L	H	H	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO B
H	L	L	H	H	L	L	H	BIT LINE IS AT L WHEN A IS AT H
H	L	L	H	H	L	L	H	A IS AT L WHEN B IS AT H
H	L	L	H	H	L	L	H	BIT LINE IS AT H WHEN A IS AT H
H	L	L	H	H	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO A
H	L	L	H	H	L	L	H	USE SUBSEQUENT VALUE OF A AS DATA TO BE WRITTEN

FIG. 38

READ (1st PAGE)

0,1,2,3		4,5,6,7		MEMORY CELL DATA	
A	B	BIT	A	B	BIT
L	L	BIT	A=LAT(A)	B=LAT(B)	BIT=BL
L	L	H	01234557	AT d	
L	L	H	BIT	READ	

FIG. 39A

READ (2nd PAGE)

0,1		2,3		4,5		6,7		MEMORY CELL DATA	
A	B	BIT	A	B	BIT	A	B	BIT	A=LAT(A), B=LAT(B), BIT=BL
L	L	BIT	L	L	BIT	L	L	BIT	READ AT f
L	L	L	L	L	L	L	L	L	POTENTIAL OF BIT1 LINE IS APPLIED TO A
L	L	L	L	L	H	L	L	H	READ AT b
L	L	L	L	L	H	L	L	H	POTENTIAL OF BIT1 LINE IS APPLIED TO A
L	L	L	L	L	H	L	L	H	BIT LINE IS AT L WHEN A IS AT H (VRFY1)
L	L	L	L	L	H	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO A

FIG. 39B

READ (3rd PAGE)

0	1	2	3	4	5	6	7	MEMORY CELL DATA
A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A=LAT(A), B=LAT(B), BIT=BL
L	L	L	L	L	L	L	H	READ AT g
L	L	L	L	L	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO A
L	L	L	L	L	L	L	H	READ AT e
L	L	L	L	L	L	L	H	BIT LINE IS AT L WHEN A IS AT H (VRFY1)
L	L	L	L	L	L	L	L	POTENTIAL OF BIT LINE IS APPLIED TO A
L	L	L	L	L	L	L	H	READ AT c
L	L	L	L	L	L	L	H	BIT LINE IS AT L WHEN A IS AT H
L	L	L	L	L	L	L	H	POTENTIAL OF BIT LINE IS APPLIED TO A
L	L	L	L	L	L	L	H	READ AT a
L	L	L	L	L	L	L	L	BIT LINE IS AT L WHEN A IS AT H (VRFY1)
L	L	L	L	L	L	L	L	POTENTIAL OF BIT LINE IS APPLIED TO A

FIG.40

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	DATA TO BE WRITTEN AND READ		
		1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN 0V	<u>1</u>	1	1
1	0.3V~0.5V	0	<u>1</u>	1
2	0.8V~1.0V	0	0	<u>1</u>
3	1.3V~1.5V	<u>0</u>	0	0
4	1.8V~2.0V	1	0	<u>0</u>
5	2.3V~2.5V	1	0	<u>1</u>
6	2.8V~3.0V	<u>1</u>	1	0
7	3.3V~3.5V	0	1	0

FIG. 41